wherein the outer periphery portion surrounds the cell portion, and

wherein the embedded second conductive type region is not disposed in the second conductive type regions of the outer periphery portion.

8. The semiconductor device according to claim **1**, further comprising:

a plurality of trenches penetrating the channel layer and reaching the first conductive type regions,

wherein the trenches have a stripe pattern,

wherein the gate insulation film is disposed on an inner wall of each trench,

wherein the gate electrode is disposed on the gate insulation film in each trench,

wherein the trenches, the gate insulation film and the gate electrode provide a trench gate structure,

wherein the first conductive type layer contacts a sidewall of each trench, and

wherein the embedded second conductive type region has an impurity concentration equal to the second conductive type regions at a position, which is deeper than a bottom of the trenches.

9. The semiconductor device according to claim **8**,

wherein the embedded second conductive type region is disposed between adjacent two trenches.

10. The semiconductor device according to claim **8**, further comprising:

an electric field relaxation layer disposed in a corresponding first conductive type region,

wherein the electric field relaxation layer contacts a bottom of a corresponding trench.

11. The semiconductor device according to claim **10**,

wherein the electric field relaxation layer has a width in the second direction, which is smaller than a width of the corresponding trench in the second direction.

12. The semiconductor device according to claim **8**,

wherein each trench extends in the first direction,

wherein the first conductive type layer extends in the first direction,

wherein the contact second conductive type region is disposed between the first conductive type layer contacting one trench and the first conductive type layer contacting an adjacent trench,

wherein the contact second conductive type region is divided into a plurality of contact second conductive type region portions along with the first direction,

wherein the contact second conductive type region portions are separated from each other by a predetermined interval, and

wherein a distance between the first conductive type layer contacting the one trench and the first conductive type layer contacting the adjacent trench, which are disposed in the predetermined interval, is shorter than a distance between the first conductive type layer contacting the one trench and the first conductive type layer contacting the adjacent trench, which sandwich a corresponding contact second conductive type region portion.

13. The semiconductor device according to claim **8**,

wherein the trenches include first to third trenches, which are adjacent to each other,

wherein the embedded second conductive type region and the contact second conductive type region are arranged between the first and second trenches, and

wherein the contact second conductive type region and the first conductive type layer are arranged between the second and third trenches.

14. The semiconductor device according to claim **8**,

wherein the contact second conductive type region and the trenches extend in the second direction, which is perpendicular to the first direction, and

wherein the embedded second conductive type region extends in the first direction.

15. The semiconductor device according to claim **14**,

wherein the embedded second conductive type region is divided into a plurality of embedded second conductive type region portions along with the first direction,

wherein the embedded second conductive type region portions are separated from each other by a predetermined interval, and

wherein each embedded second conductive type region portion is disposed under the contact second conductive type region.

16. The semiconductor device according to claim **10**, further comprising:

a cell portion; and

an outer periphery portion,

wherein the current flows between the surface electrode and the backside electrode in the cell portion,

wherein the outer periphery portion surrounds the cell portion,

wherein the trenches in the cell portion extend in the first direction,

wherein the embedded second conductive type region in the cell portion and the outer periphery portion extends in the first direction, and

wherein the embedded second conductive type region has an end in the outer periphery portion, which is disposed on an outer side of an end of the trench in the first direction.

17. The semiconductor device according to claim **16**,

wherein the embedded second conductive type region is divided into a plurality of embedded second conductive type region portions along with the first direction, and

wherein the embedded second conductive type region portions are separated from each other by a predetermined interval.

18. A method for manufacturing a semiconductor device comprising:

forming a first conductive type region film on a substrate having a first conductive type;

forming a plurality of first trenches on the first conductive type region film to reach the substrate so that the first conductive type region film is divided into a plurality of first conductive type regions, which are separated from each other with the first trenches;

filling each first trench with a second conductive type region film;

polishing a surface of the second conductive type region film so that the second conductive type region film is divided into a plurality of second conductive type regions, and the first conductive type regions and the second conductive type regions provide a super junction structure, wherein the first conductive type regions and the second conductive type regions extend in a first direction, and wherein the first conductive type regions and the second conductive type regions are alternatively arranged in a second direction;